

**SYSTEM AND METHOD FOR ERASING
HIGH-DENSITY NON-VOLATILE FAST MEMORY**

BACKGROUND

5 EEPROMs, as is known in the art, require specialized on-chip circuitry to electrically discharge their floating gates. Additionally, since the discharging circuitry is attached to the floating gate transistors on a byte-by-byte basis, the complexity of the chip increases proportionally with an increase in the number of bytes in the EEPROM. Furthermore, since the memory cells of the EEPROM are written and erased at the byte 10 level, the updating of memory in EEPROM is a relatively slow process.

 In order to remedy the problem associated with EEPROM, the industry responded with high-density non-volatile fast memory, such as flash memory. Unlike the EEPROM memory, the erasing circuitry in flash memory is moved to the periphery of the memory array. The location of the erasing circuitry at the periphery of the memory permits 15 erasure of entire blocks of data using in-circuit wiring. Thus, rather than erasing byte-by-byte, flash memory is erased and rewritten in large blocks of, for example, 8 kilobytes (K) to 128K. The block erasure and rewriting of flash memory results in faster performance of flash memory when compared to the performance of the EEPROM. Additionally, by moving the erasing circuitry to the periphery of the memory array, greater chip density is 20 achievable than that of the EPROM or the EEPROM. Moreover, different configurations of flash memory (*e.g.*, NAND configurations and NOR configurations) allow for rearrangement of a bit line and a word line. The rearrangement of bit lines and word lines permits balancing of chip density with chip processing speed.

 Unfortunately, the complexity of the erasing circuitry is still present due to the 25 nature of flash memory. Furthermore, a relatively high voltage is typically required to

erase flash memory. Also, the aggregate cost of the erasing circuitry in flash memory is fairly significant, thereby making flash memory relatively expensive.

In view of the deficiencies associated with flash memory, a need exists in the art.

5 **SUMMARY**

The present disclosure provides systems and methods for erasing high-density non-volatile fast memory, such as modified flash cells.

Briefly described, in architecture, one embodiment of the system comprises modified flash cells, which have no erasing circuitry, and an ultraviolet (UV) light window. The UV light window is adapted to expose the modified flash cells to UV light.

10 The present disclosure also provides methods for erasing high-density non-volatile fast memory. In this regard, one embodiment of the method comprises the steps of exposing a modified flash cell to ultraviolet (UV) light, and erasing the modified flash cell using the UV light.

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BRIEF DESCRIPTION OF THE DRAWINGS

Many aspects of the disclosure can be better understood with reference to the following drawings. The components in the drawings are not necessarily to scale.

20 FIG. 1A is a diagram illustrating a modified flash cell having a window for ultraviolet (UV) light.

FIG. 1B is a diagram illustrating a two-terminal drain-gate-connected modified flash cell having a window for UV light.

FIG. 2 is a block diagram illustrating a plurality of modified flash cells having UV light windows.

FIG. 3 is a block diagram showing a top view of a modified flash memory array having UV light windows.

FIG. 4A is a circuit diagram of a modified flash memory array having UV light windows above the control gates of the floating gate transistors.

5 FIG. 4B is a circuit diagram of a modified flash memory array having UV light windows below the substrate of the floating gate transistors.

FIG. 4C is a circuit diagram of a modified flash memory array having UV light windows between the control gates of the floating gate transistors.

FIG. 5 is a block diagram showing a top view of a modified flash memory having
10 UV light windows directly above the control gate of the floating gate transistors.

FIG. 6 is a block diagram showing a top view of a modified flash memory having UV light windows offset from the control gate of the floating gate transistors.

FIG. 7 is a flowchart showing one embodiment of the method of the invention.

FIG. 8 is a diagram showing a cellular telephone having a UV light window.

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DETAILED DESCRIPTION

Reference is now made in detail to the description of the embodiments as illustrated in the drawings.

In order to provide simpler circuitry in high-density non-volatile fast memory
20 (e.g., modified flash cells as described with reference to FIG. 1A, and two-terminal drain-gate-connected modified flash cells as described with reference to FIG. 1B), erasing circuitry is removed from the chip and replaced with windows that permit the entry of ultraviolet (UV) light. The UV light excites electrons on the floating gates of the high-density non-volatile fast memory and erases the circuit without the need for erasing
25 circuitry. While UV light is specifically described herein, it should be appreciated that

other types of radiation may be used so long as that radiation is sufficient to excite the electrons on the floating gate.

FIG. 1A is a diagram illustrating a high-density non-volatile fast memory 610 having windows 620 for UV light (hereinafter "UV light windows"). For simplicity, the 5 high-density non-volatile fast memory 610 having three terminals is referred to herein as a modified flash cell 610.

The modified flash cell 610 comprises a control gate 430, a floating gate 440, and an inter-poly (IP) oxide layer that separates the control gate 430 from the floating gate 440. Furthermore, the modified flash cell 610 comprises a positively-doped silicon 10 substrate 510 (hereinafter "p-type substrate") and a field oxide layer 530 that separates the floating gate 440 from the p-type substrate 510. Additionally, the modified flash memory 610 comprises a negatively-doped source (hereinafter "n+ source") 630 and a negatively-doped drain (hereinafter "n+ drain") 550. As shown in FIG. 1A, the configuration of the n+ source 630 is different from the configuration of a standard flash cell. Unlike the 15 standard flash cell in which the n+ source 560 overlaps with the floating gate 440, the n+ source 630 in the modified flash cell 610 does not overlap with the floating gate 440. The removal of overlap between the n+ source 630 and the floating gate 440 eliminates the ability to electrically erase the modified flash cell 610. The erasure, therefore, is accomplished by exposing the modified flash cell 610 to ultraviolet (UV) light through a 20 UV light window 620. In the embodiment of FIG. 1A, the UV light window 620 is placed directly over the control gate 430. Also, in one embodiment, the UV light windows 620 are configured to diffuse the light, thereby globally irradiating the modified flash cells 610 with UV light. The diffusing of light may be accomplished by using 25 frosted glass or other apparatuses known to diffuse light such as, for example, diffraction gratings.

In addition to removing complicated erasing hardware, the removal of the overlap between the n+ source 630 and the floating gate 440 provides a relaxed dimension constraint between source and drain regions. Removal of this overlap provides greater scalability to smaller geometries. In other words, an increased chip density may be 5 achieved by removing the overlapping region between the n+ source 630 and the floating gate 440.

FIG. 1B is a diagram illustrating a high-density two-terminal non-volatile memory cell 615 (hereinafter "two-terminal drain-gate-connected modified flash cell"). The two-terminal drain-gate-connected modified flash cell 615 may be a modified nitrided read-only memory (NROM) having the source and gate electrically shorted so that electrons 10 are only stored on the drains side. In other words, a two-terminal drain-gate-connected modified flash cell 615 may be derived by diode connecting the NROM cell. As shown in FIG. 1B, the two-terminal drain-gate-connected modified flash cell 615 comprises a first oxide layer 645, a nitride layer 650, and a second oxide layer 655 that substitute for 15 the field oxide 530 and the floating gate 440 of a modified flash cell. The first oxide layer 645, the nitride layer 650, and the second oxide layer 655 are known in the aggregate as the oxide-nitride-oxide (ONO) layer. Since, as shown in FIG. 1B, the drain and the gate are electrically shorted, the two-terminal drain-gate-connected modified flash cell 615 exhibits diode-like behavior. Thus, the two-terminal drain-gate-connected 20 modified flash cell 615 is programmed by channel hot-electron injection, similar to the process of programming the modified flash cell 610 of FIG. 1A.

Erasure of the two-terminal drain-gate-connected modified flash cell 615 is accomplished by exposing the two-terminal drain-gate-connected modified flash cell 615 to ultraviolet (UV) light through a UV light window 620. In the embodiment of FIG. 1B, 25 the UV light window 620 is placed over the two-terminal drain-gate-connected modified

flash cell 615. Furthermore, the UV light window 620 may be configured to diffuse the light similar to that described with reference to FIG. 1B.

FIG. 2 is a block diagram illustrating a plurality of modified flash cells 610 having UV light windows 620. As shown in FIG. 2, the embodiment of FIG. 1A may be

5 extended to a plurality of modified flash cells 610. Thus, as shown in FIG. 2, each flash cell 610 has a UV light window 620 placed directly over the control gate 430 of the modified flash cell 610. While only a one-dimensional array is shown in FIG. 2, the one-dimensional array may further be expanded to a two-dimensional planar configuration, or even to a three-dimensional layered configuration. This embodiment is described in
10 greater detail in FIGS. 5 and 6. While not specifically shown in FIG. 2, the two-terminal drain-gate-connected modified flash cells 615 of FIG. 1B may also be extended to a plurality of cells.

FIG. 3 is a block diagram showing a top view of a modified flash memory array having UV light windows. Specifically, a modified NAND flash array with UV light

15 windows 620 is shown in FIGS. 3 through 6. The modified NAND flash array comprises a bit line 130, a bit line contact 820, a select gate 830, a control gate 430, a floating gate 440, and a source line 420. As seen from the top-view of FIG. 3, the select gate 830 and the modified flash cells 610 are configured to be perpendicular to the bit line 130. Thus, the select gate 830 is adapted to select the modified flash cells 610 in the entire bit line
20 830, and appropriate word lines (not shown in FIG. 3) are adapted to select the individual modified flash cells 610 attached to the bit line 130. The floating gates 440 of the modified flash cells 610 are located above the bit line 130, and the control gates 430 of the modified flash cells 610 are located above their respective control gates 430. The UV light window 620 is located above the modified flash cells 610, and permits UV light to
25 access the floating gate 440. While not specifically shown in FIG. 3, the two-terminal

drain-gate-connected modified flash cells 615 of FIG. 1B may also be configured as a NAND array having a UV window 620.

FIG. 4A is a circuit diagram of the modified flash memory array from FIG. 3. As shown in FIG. 4A, the modified flash memory array has UV light windows 620 above the 5 control gates 430 of the modified flash cells 610. Thus, when UV light enters the UV light windows 620, the UV light excites the electrons that are trapped on the floating gate 440. The excitation of the electrons provides enough energy to the electrons to migrate from the floating gate 440 back to the n+ source (not shown in FIG. 4A).

FIG. 4B is a circuit diagram of another embodiment of a modified flash memory 10 array having UV light windows 620. Unlike the embodiment of FIG. 4A, the UV light windows 620 in the embodiment of FIG. 4B are placed underneath the substrate, rather than above the control gate 430. Thus, in the embodiment of FIG. 4B, the modified flash cells 610 are irradiated with UV light from beneath the circuit, rather than from above the circuit as in FIG. 4A. Once the energy (hereinafter "UV energy") from the UV light 15 diffuses into the floating gates 610, the UV energy excites the electrons, which migrate from the floating gates 430 back to the n+ source.

FIG. 4C is a circuit diagram of yet another embodiment of a modified flash memory array having UV light windows. Unlike the embodiments of FIGS. 4A and 4B, the UV light windows 620 in the embodiment of FIG. 4C are placed between the control 20 gates 430 of the modified flash cells 610. Thus, if light-diffusing windows are used for the UV light windows 620, then the UV light entering the UV light windows globally irradiates the modified flash cells 610 and permits the UV energy to diffuse transversely into the floating gates 440. Once the UV energy diffuses into the floating gates 610, the UV energy excites the electrons, and the excited electrons migrate back to the n+ source 25 from the floating gates 430.

While not specifically shown in FIGS. 4A through 4C, the two-terminal drain-gate-connected modified flash cells 615 of FIG. 1B may also be arranged in similar fashion.

FIG. 5 is a block diagram showing a top view of one embodiment of a modified 5 flash memory. In the embodiment of FIG. 5, the memory has UV light windows 620 directly above the control gates 430 of the modified flash cells 610. Unlike the embodiment of FIG. 3, which is a one-dimensional array of a modified NAND flash memory, the embodiment of FIG. 5 is a two-dimensional planar configuration of a modified NAND flash memory. As shown in FIG. 5, each of the modified flash cells 610 are located at the juncture of a word line 120 and a bit line 130. Thus, for example, a 10 specific modified flash cell 610 may be write-accessed or read-accessed through the appropriate word line 120 and the appropriate bit line 130.

Given this configuration, when UV light enters the UV light windows 620, the 15 UV light excites the electrons that are trapped on the floating gate 440. The excitation of the electrons provides enough energy for the electrons to migrate from the floating gate 440 back to the n⁺ source (not shown in FIG. 5).

While only one layer of memory is shown in FIG. 5, additional layers may be 20 provided to increase memory capacity. Thus, for modified flash cells 610 configured as multiple layers, the exposure of UV energy through the UV light windows 620 excites the electrons that are trapped on the floating gates 440 at the various layers. The excitation of the electrons provides enough energy for the electrons to migrate from the floating gate 440 of the various layers back to the n⁺ source (not shown in FIG. 5) at the various layers.

FIG. 6 is a block diagram showing a top view of another embodiment of a 25 modified flash memory. In the embodiment of FIG. 6, the memory has UV light

windows 620 that are offset from the control gate 440 of the modified flash cells 610. In this regard, rather than having the UV light directly hit the control gate 440, the embodiment of FIG. 6 permits UV energy to transversely diffuse into the modified flash cells 610. Thus, once the UV energy enters through the UV light windows 620 and 5 transversely diffuses to the floating gates 440, the UV energy excites the electrons that are trapped on the floating gates 440. The excitation of the electrons provides enough energy for the electrons to migrate from the floating gate 440 back to the n+ source (not shown in FIG. 6).

While only one layer of memory is shown in FIG. 6, additional layers may be 10 provided to increase memory capacity. Thus, for modified flash cells 610 configured as multiple layers, UV energy diffuses through the UV light windows 620 and the various layers, thereby exciting the electrons that are trapped on the floating gates 440 at the various layers. The excitation of the electrons provides enough energy for the electrons to migrate to the n+ source (not shown in FIG. 6) from the floating gate 440 of the 15 various layers.

Also, while not specifically shown in FIGS. 5 and 6, the two-terminal drain-gate-connected modified flash cells 615 of FIG. 1B may also be configured as a two-dimensional planar matrix or as three-dimensional layers.

As shown in FIGS. 1A through 6, the need for erasing circuitry may be eliminated 20 by having UV light windows 620 that expose the modified flash cells 610 to UV light. Additionally, unlike the UV erasable EPROMS of the prior art, by using modified flash cells 610, a much greater chip density may be achieved, and, also, much faster chips may be built as compared to conventional UV erasable EPROMS. Moreover, if the modified flash cells 610 having the UV light windows 620 are used in portable devices such as cell 25 phones or personal digital assistants (PDA), then the UV light windows 620 may be

directly built into these devices. Thus, the modified flash cells 610 may be erased while they are housed in the cell phone or PDA. One example of a portable device having a UV light window 620 is shown in FIG. 8. Specifically, a cell phone 800 is shown in FIG. 8 as the portable device having the UV light window 620.

5 While FIGS. 1A through 6 show several embodiments of a system for erasing high-density non-volatile fast memory (*e.g.*, modified flash cells 610, or two-terminal drain-gate-connected modified flash cells 615), another embodiment may be seen as a method for erasing high-density non-volatile fast memory. One embodiment of the method is shown in FIG. 7.

10 FIG. 7 is a flowchart showing a method for erasing high-density non-volatile fast memory. As shown in FIG. 7, one embodiment of the method comprises exposing (1220) a high-density non-volatile fast memory to UV light, and erasing (1230) the high-density non-volatile fast memory using the UV light. The high-density non-volatile fast memory may be a modified flash memory (*e.g.*, the modified flash cell of FIG. 1A), or a two-terminal drain-gate-connected modified flash memory (*e.g.*, the two-terminal drain-gate-connected modified flash of FIG. 1B).

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Although exemplary embodiments have been shown and described, various changes, modifications, or alterations may be made. For example, while an example of a NAND array is shown in the drawings, a NOR flash array may be used. Furthermore, 20 while specific embodiments are shown using modified flash memories and two-terminal drain-gate-connected modified flash memories, other high-density non-volatile fast memories may be compatible with the embodiments described herein. Furthermore, while specific embodiments are shown with multiple UV light windows at various locations with reference to the control gates, a single large UV light window or several 25 smaller UV light windows may be used to irradiate the entire memory chip with UV

energy. Also, while cell phones and PDA devices have been provided as example environments in which modified flash cells may be used, the modified flash cells may be used in any electronic device that uses high-density non-volatile fast memory, such as, for example, an MP3 player or a portable computer. All such changes, modifications, and 5 alterations should therefore be seen as within the scope of the present disclosure.